

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Gated Semiconductor Assemblies And Methods Of Forming Gated Semiconductor Assemblies, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * *

Full name of inventor: Mark A. Helm

Inventor's Signature: Mark A. Helm

Date: 3/26/98

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* * * * *

Full name of inventor: Mark Fischer

Inventor's Signature: Mark Fischer

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* * * * *

Full name of inventor: John T. Moore

Inventor's Signature: John T. Moore

Date: 3/24/98

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Full name of inventor: Scott Jeffrey DeBoer

Inventor's Signature: Scott J DeBoer

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. Unknown
 Filing Date Unknown
 Inventor Mark A. Helm, et al
 Assignee Micron Technology, Inc.
 Group Art Unit Unknown
 Examiner Unknown
 Attorney's Docket No. MI22-845
 Title: Gated Semiconductor Assemblies And Methods of Forming Gated
 Semiconductor Assemblies

POWER OF ATTORNEY BY ASSIGNEE AND
CERTIFICATE BY ASSIGNEE UNDER 37 CFR §3.73(b)

To: Assistant Commissioner for Patents
 Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., the Assignee of the entire right,
 title and interest in the above-identified patent application by assignment
 attached hereto, hereby appoints the attorneys and agents of the firm
 of WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., listed
 as follows:

Richard J. St. John	Reg. No. 19,363
David P. Roberts	Reg. No. 23,032
Randy A. Gregory	Reg. No. 30,386
Mark S. Matkin	Reg. No. 32,268
James L. Price	Reg. No. 27,376
Deepak Malhotra	Reg. No. 33,560
Mark W. Hendricksen	Reg. No. 32,356
David G. Latwesen	Reg. No. 38,533
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Keith D. Grzelak	Reg. No. 37,144
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James D. Shaurette	Reg. No. 39,833

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia Pappas
 Dennison (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys

1 with full power of substitution to prosecute this application and transact
2 all business in the Patent and Trademark Office connected therewith.

3 The Assignee certifies that the above-identified Assignment has
4 been reviewed and to the best of Assignee's knowledge and belief, title
5 is in the Assignee.

6 Please direct all correspondence regarding this application to:

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13 MICRON TECHNOLOGY, INC.

14 Dated: Mar 31, 1988

By: [Signature]

15 Name: Michael L. Lynch

16 Title: Chief Patent Counsel